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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,861	01/05/2001	Lewis A. Morrow	YOR9-2000-0472US1 (8728-4	3687

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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,861	MORROW ET AL.	
	Examin r	Art Unit	
	Paul B Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant should note that the references relied upon by the examiner in the first office action (dated 11/19/2003) have been reconsidered in view of the Applicant's arguments. The examiner has determined that the combination of the Cai and Inoue references as more fully explained below does disclose the claimed subject matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cai, US Patent no. 6,501,999[1], in view of, Inoue, US Patent no. 4,954,945[2].

Regarding claims 1 and 11, Cai teaches a computer system comprising:

at least two processing units [high-performance processor and power-efficient processor] having different energy efficiencies and adapted to at least execute tasks based on processing requirements of the tasks and a corresponding processing capablility [column 2, lines 46-67]; and

a scheduler [processor arbitration mechanism] adapted to schedule a given task for execution by one of said at least two processing units so as to consume a least amount of energy, and to reschedule the given task for execution by another of said at least two processing units when a determination indicates that one of said at least two processing units is unable to

accommodate execution of the given task based upon the processing requirements of the given task and the corresponding processing capability [column 3, lines 25-48].

Cai teaches a scheduler [processor arbitration mechanism], which, during battery operation mode, attempts to schedule tasks for execution on the power-efficient processor until it determines that the high-performance processor is needed to execute a particular task, such as processing graphic data. The high-performance processor is then powered up to execute the task [column 3, lines 25-48].

Cai does not explicitly teach that the processors are adapted to accept and reject tasks for execution. Inoue teaches a method of selecting a processor to execute a particular task in a multi-processor system, in which each processor is queried about whether it is able to execute a task. Each processor then outputs a corresponding accept or reject signal reflecting its ability to process the task. If more than one processor is capable of executing the task then the most efficient processor is selected [column 3, lines 22-45].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Cai and Inoue. Enabling each processor to determine whether or not it can successfully execute a process according to certain requirements would allow for less complex task scheduling circuitry since the task scheduling circuitry would no longer need to determine processor capabilities.

Regarding claim 2, it is inherent in the teachings of Cai and Inoue that the task execution end time is considered when analyzing the processing requirements for the task. Cai teaches that tasks concerning processing graphic data require a high-performance processor for execution. It

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[1] included in previous office action dated 11/19/2003.

is essential that graphical data be processed by a certain time so it can be displayed to a user without a noticeable delay.

Regarding claims 3 and 4, Cai teaches that the processor arbitration logic is part of host interface circuitry. Cai teaches that the host interface logic may be on the same die as the power efficient processor. Therefore Cai suggests that the processor arbitration logic may be embodied within the same hardware component as one of the processors or within a separate hardware component [column 4, lines 27-35 and Figure 1].

Regarding claims 5-7, Cai teaches that the two processors share system memory and I/O space and use the host interface to access the shared memory, I/O space and PCI bus [column 4, lines 5-35 and Figure 1].

Regarding claim 8, Cai teaches that the two processors and the host interface share system memory and I/O space [column 4, lines 5-35 and Figure 1].

Regarding claim 9, it is inherent that some type of task attribute store would have to be used by the processor arbitration logic in order to successfully identify which tasks require high-performance processing and which tasks can be executed on the power efficient processor.

Regarding claim 10, Cai teaches that the processor arbitration mechanism determines when the power-efficient processor is not capable of executing a particular task [column 3, lines 25-35].

Regarding claim 13, Cai teaches that the processor arbitration mechanism selects the proper processor based on predetermined criteria, such as processing power [column3, lines 35-45].

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[2] included in previous office action dated 11/19/2003.

Regarding claim 14, Cai teaches a computer system comprising:

a plurality of processing units [high-performance processor and power-efficient processor], each of the plurality of processing units adapted to execute tasks thereon, and at least two of the plurality of processing units having different energy efficiencies [column 2, lines 46-67]; and

a scheduler [processor arbitration mechanism] adapted to schedule a given task for execution by one of said plurality of processing units.

Cai does not explicitly teach querying the processing units to accept or reject a particular task. Inoue teaches a method of selecting a processor to execute a particular task in a multi-processor system, in which each processor is queried about whether it is able to execute a task. Each processor then outputs a corresponding accept or reject signal reflecting its ability to process the task. If more than one processor is capable of executing the task then the most efficient processor is selected [column 3, lines 22-45].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Cai and Inoue. Enabling each processor to determine whether or not it can successfully execute a process according to certain requirements would allow for less complex task scheduling circuitry since the task scheduling circuitry would no longer need to determine processor capabilities.

Regarding claims 15 and 16, Cai teaches that the processor arbitration logic is part of host interface circuitry. Cai teaches that the host interface logic may be on the same die as the power efficient processor. Therefore Cai suggests that the processor arbitration logic may be embodied

within the same hardware component as one of the processors or within a separate hardware component [column 4, lines 27-35 and Figure 1].

Regarding claims 17-19, Cai teaches that the two processors share system memory and I/O space and use the host interface to access the shared memory, I/O space and PCI bus [column 4, lines 5-35 and Figure 1].

Regarding claim 20, Cai teaches that the two processors and the host interface share system memory and I/O space [column 4, lines 5-35 and Figure 1].

Regarding claim 21 and 23, it is inherent that some type of task attribute store would have to be used by the processor arbitration logic in order to successfully identify which tasks require high-performance processing and which tasks can be executed on the power efficient processor.

Regarding claim 22, Inoue teaches excluding processors that are currently busy and not able to process a task [column 3, lines 39-43].

Regarding claim 24, Cai teaches a computer system comprising:

at least two processing units [high-performance processor and power-efficient processor] having different energy efficiencies and adapted to at least execute tasks based on processing requirements of the tasks and a corresponding processing capability [column 2, lines 46-67]; and

a scheduler [processor arbitration mechanism] adapted to schedule a given task for execution by one of said at least two processing units so as to consume a least amount of energy, and to rescheduled the given task for execution by an other of said at least two processing units when said one of said at least two processing units rejects the execution of the given task [column 3, lines 25-48].

Cai does not explicitly teach querying the processing units to accept or reject a particular task. Inoue teaches a method of selecting a processor to execute a particular task in a multi-processor system, in which each processor is queried about whether it is able to execute a task. Each processor then outputs a corresponding accept or reject signal reflecting its ability to process the task. If more than one processor is capable of executing the task then the most efficient processor is selected [column 3, lines 22-45].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Cai and Inoue. Enabling each processor to determine whether or not it can successfully execute a process according to certain requirements would allow for less complex task scheduling circuitry since the task scheduling circuitry would no longer need to determine processor capabilities.

Regarding claims 25 and 26, Cai teaches that the processor arbitration logic is part of host interface circuitry. Cai teaches that the host interface logic may be on the same die as the power efficient processor. Therefore Cai suggests that the processor arbitration logic may be embodied within the same hardware component as one of the processors or within a separate hardware component [column 4, lines 27-35 and Figure 1].

Regarding claims 27-29, Cai teaches that the two processors share system memory and I/O space and use the host interface to access the shared memory, I/O space and PCI bus [column 4, lines 5-35 and Figure 1].

Regarding claim 30, Cai teaches that the two processors and the host interface share system memory and I/O space [column 4, lines 5-35 and Figure 1].

Regarding claim 31, Cai teaches a computer system comprising:

a plurality of processing units, each of the plurality of processing units adapted to execute tasks thereon, and at least two of the plurality of processing units having different energy efficiencies; and

a scheduler adapted, for a given task, to retrieve at least some of the processing capability information from said processor attribute table in one of a partial order and a strict order of descending energy efficiency until one of the plurality of processors is found to possess adequate processing capability with respect to task processing requirements for the given task, and to schedule the given task for execution by said one of the plurality of processors.

Cai does not explicitly teach a processor attribute table adapted to store processing capability information for at least some of said plurality of processors and to update the processing capability information dynamically when the processing capability information changes. Inoue teaches storing a table of tasks, which can be performed by the processor and a flag value to indicate if the processor is currently busy [column 3, lines 20-60 and Figure 4]. Since the table stores an indication of whether the processor is currently busy, the table must be updated dynamically.

Regarding claim 32, Cai teaches generating an interrupt to allow the power-efficient processor to take over execution of the high-performance processor [column 4, lines 53-60].

Regarding claim 33, Cai teaches a graphics controller which would be used by a graphics data processing task [column 4, lines 19-26].

Response to Arguments

Applicant's arguments with respect to claims 1-11 and 13-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
January 10, 2005

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SUPERVISORY PATENT EXAMINER
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